IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: KAJIHARA, et al.

Serial No.: 09/989,242

Filed: November 21, 2001

For: LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: 2815

Examiner: Jasmine Jhihan B Clark

Conf. No.: 9603

PETITION FOR WITHDRAWAL OF ERRONEOUS HOLDING OF ABANDONMENT

Mail Stop: Amendment (No Fee)
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 3, 2010

Sir:

Applicant, through its undersigned attorney, acknowledges receipt of a notice of abandonment mailed December 18, 2009, in connection with the above-identified application. However, since the notice of abandonment is in error, withdrawal of the erroneous holding of abandonment is requested.

The notice of abandonment indicates the application to be abandon for failure to respond to the office action of May 14, 2009. However, a response to the office action was filed on November 16, 2009 with appropriate extension fees. A copy of the Amendment, Extension of Time and Electronic Acknowledgement Receipt from the US Patent Trademark Office, evidencing receipt of the Amendment in the United States Patent and Trademark Office on November 16, 2009 are attached. Since the

response was timely filed, the notice of abandonment is in error and should be withdrawn.

Please charge any shortage in the fees due in connection with the filing of this paper, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case No. 1374.32049RV2), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

/Paul J. Skwierawski/
Paul J. Skwierawski
Registration No. 32,173

PJS/slk
(703) 312-6600
Attachments

Electronic Acknowledgement Receipt

EFS ID:	6460555
Application Number:	09989242
International Application Number:	
Confirmation Number:	9603
Title of Invention:	LEADFRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING THE SAME AND METHOD OF AND PROCESS FOR FABRICATING THE TWO
First Named Inventor/Applicant Name:	Yujiro Kajihara
Customer Number:	20457
Filer:	Paul J. Skwierawski/Stacey Keaton
Filer Authorized By:	Paul J. Skwierawski
Attorney Docket Number:	1374.32049RV2
Receipt Date:	16-NOV-2009
Filing Date:	21-NOV-2001
Time Stamp:	15:37:42
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Amendment/Req. Reconsideration-After Non-Final Reject	32049RV2amd.pdf	166958 d1ec70bfe8fac4d293b49c69c57090ef3e1b1ffb	no	21
Warnings:					
Information:					
2	Extension of Time	32049RV2eot.pdf	56582 ffed86fdecd0794276c53b7fd96e5a3ab8361 87f	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30948 7767ee34ab932f65bfdb0243987b818e0aff 9702	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	254488	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

1374.32049RV2 / 329201392US5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: KAJIHARA, et al.

Serial No.: 09/989,242

Filed: November 21, 2001

For: LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: 2815

Examiner: Jasmine Jhihan B Clark

Conf. No.: 9603

PETITION FOR EXTENSION OF TIME

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

November 16, 2009

Sir:

In the matter of the above-identified application, applicants hereby respectfully petition for an extension of time to permit filing a response within the third month subsequent to expiration of the shortened statutory period set in the outstanding Office Action mailed May 14, 2009. An electronic payment in the amount of $1,110.00 to cover the required fee for the requested extension of time is being submitted herewith.

It is respectfully requested that any shortage in the fee be charged to the account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (Case No. 1374.32049RV2).

Respectfully submitted,
ANTONELLI, TERRY STOUT & KRAUS, LLP

/Paul J. Skwierawski/
Paul J. Skwierawski
Registration No. 32,173

PJS/slk

1374.32049RV2 / 329201392US5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: KAJIHARA, et al.

Serial No.: 09/989,242

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For: LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: 2815

Examiner: Jasmine Jhihan B Clark

Conf. No.: 9603

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

November 16, 2009

Sir:

In response to the Office Action dated May 14, 2009, please amend the above-identified application as listed below and as set forth on the following pages:

Amendments to the Claims

Remarks are included following the amendments

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-36. (Cancelled)

37. (Three Times Amended) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads; and

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to at least said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and at least a portion of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said insulating tape has a frame shape and is continuously formed between said suspension leads and said plurality of leads,

wherein said chip mounting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is fixed to said chip mounting portion by an adhesive,

wherein said semiconductor chip is fixed to a part of each of suspension leads by an adhesive, and

wherein said suspension leads and said chip mounting portion of said lead frame are continuously formed in an area of said semiconductor chip.

38. (Unamended) A semiconductor device according to Claim 37, wherein said resin member has a rectangular shape, wherein said suspension leads extend from said chip mounting portion toward four corners of said resin member, and wherein said plurality of leads are arranged between said suspension leads in a plane view.

39. (Unamended) A semiconductor device according to Claim 37, wherein said insulating tape extends along four sides of said resin member to surround said chip mounting portion and said semiconductor chip in a plane view.

40. (Three Times Amended) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads; and

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to at least said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and at least a portion of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said insulating tape has a frame shape and is continuously formed between said plurality of leads and said suspension leads,

wherein said insulating tape includes a base insulating film and an adhesive layer applied to one surface of said base insulating film, and

wherein said insulating tape is adhered to said plurality of leads and said suspension leads by said adhesive layer,

wherein said chip mounting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is fixed to said chip mounting portion by an adhesive,

wherein said semiconductor chip is fixed to a part of each of suspension leads by an adhesive, and

wherein said suspension leads and said chip mounting portion of said lead frame are continuously formed in an area of said semiconductor chip.

41. (Unamended) A semiconductor device according to Claim 40, wherein said base insulating film includes a polyimide resin and said adhesive layer includes an acrylic resin.

42. (Three Times Amended) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip;

a plurality of leads; and

suspension leads continuously formed with said chip mounting portion, said semiconductor chip being mounted on said chip mounting portion;

(c) an insulating tape adhered to at least said plurality of leads and said suspension leads;

(d) bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively, and

(e) a resin member sealing said semiconductor chip, said bonding wires, said insulating tape, said chip mounting portion, a part of each of said suspension leads, and at least a portion of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said insulating tape has a frame shape and is continuously formed between said plurality of leads and said suspension leads,

wherein said lead frame having a first surface and a second surface opposite to said first surface, wherein each of said suspension leads has a step portion so that said first surface of said chip mounting portion is positioned to the side of said second surface of said plurality of leads rather than the side of said first surface of said plurality of leads, and

wherein said insulating tape is arranged outside said step portion of each of said suspension leads,

wherein said chip mounting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is fixed to said chip mounting portion by an adhesive,

wherein said semiconductor chip is fixed to a part of each of suspension leads by an adhesive, and

wherein said suspension leads and said chip mounting portion of said lead frame are continuously formed in an area of said semiconductor chip.

43. (Unamended) A semiconductor device according to Claim 43, wherein a part of each of said suspension leads, which is located outside said step portion, is substantially at a same level as portions of said plurality of leads in a thickness direction of said lead frame.

44. (Once Amended) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion; and

a plurality of leads;

(c) a plurality of bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing at least said semiconductor chip, said bonding wires, said chip mounting portion and at least portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is mounted on said chip mounting portion, such that said rear surface of said semiconductor chip is bonded to the side of said first surface of said chip mounting portion by an adhesive, and such that a part of each of said suspension leads, which is located under said semiconductor chip, is spaced from said rear surface of said semiconductor chip,

wherein said chip mounting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is bonded to the part of each of suspension

leads by an adhesive, and

wherein said suspension leads and said chip mounting portion of said lead frame are continuously formed in an area of said semiconductor chip.

45. (Unamended) A semiconductor device according to Claim 44, wherein said adhesive layer is provided on said first surface of said chip mounting portion and is not provided on said part of each of said suspension leads which is located under said semiconductor chip.

46. (Unamended) A semiconductor device according to Claim 45, wherein a part of said rear surface of said semiconductor chip, which is located outside said chip mounting portion, is adhered to a part of said resin member.

47. (Unamended) A semiconductor device according to Claim 46, wherein said resin member includes a thermosetting resin.

48. (Unamended) A semiconductor device according to Claim 44, wherein said adhesive layer includes an epoxy resin.

49. (Once Amended) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof and a rear surface opposite to said main surface;

(b) a lead frame having a first surface and a second surface opposite to said

first surface, said lead frame having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads continuously formed with said chip mounting portion; and

a plurality of leads;

(c) a plurality of bonding wires electrically connected to said plurality of leads with said bonding pads of said semiconductor chip respectively; and

(d) a resin member sealing at least said semiconductor chip, said bonding wires, said chip mounting portion and at least portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said semiconductor chip is bonded to said chip mounting portion by an adhesive between said rear surface of said semiconductor chip and said first surface of said chip mounting portion,

wherein each of said suspension leads has a part which is located under said semiconductor chip,

wherein a part of said resin member is formed between said part of each of said suspension leads and said rear surface of said semiconductor chip,

wherein said chip mounting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is bonded to the part of each of suspension leads by an adhesive, and

wherein said suspension leads and said chip mounting portion of said lead frame are continuously formed in an area of said semiconductor chip.

50. (Once Amended) A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a first suspension lead for supporting said semiconductor chip, extending in a first direction;

a second suspension lead for supporting said semiconductor chip, extending in a second direction which is different from said first direction, said second suspension lead intersecting said first suspension lead; and

a plurality of leads, said plurality of leads being arranged to extend toward an intersecting portion of said first and second suspension leads;

(3) a plurality of bonding wires electrically connecting at said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, at least a portion of said plurality of leads, said first and second suspension leads and said plurality of bonding wires,

wherein said semiconductor chip is disposed on said intersecting portion of said first and second suspension leads,

wherein a width of each of said first and second suspension leads at the vicinity of said intersecting portion is wider than that of each of said first and second suspension leads at vicinities beyond said semiconductor chip,

wherein said rear surface of said semiconductor chip is fixed to said first and

second suspension leads at the vicinity of said intersecting portion by an adhesive,

wherein said intersecting portion is positioned under a substantially central portion of said semiconductor chip,

wherein said semiconductor chip is bonded to a part of each of suspension leads by an adhesive, and

wherein said suspension leads and said intersecting portion of said lead frame are continuously formed in an area of said semiconductor chip.

51. (Unamended) A semiconductor device according to Claim 50, wherein said first and second suspension leads intersect each other at a substantially right angle.

52. (Unamended) A semiconductor device according to Claim 51, wherein said resin body has a tetragonal shape, wherein said plurality of leads extends toward four sides of said resin body, and wherein said first and second suspension leads extend from said intersecting portion toward four corners of said resin body.

53. (Unamended) A semiconductor device according to Claim 50, wherein a portion of said rear surface of said semiconductor chip is adhered to said intersecting portion of said first and second suspension leads, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

54. (Unamended) A semiconductor device according to Claim 51, wherein said semiconductor chip has a tetragonal shape, and wherein said wider portion at

the vicinity of said intersecting portion of said first and second suspension leads extends from a central portion of said rear surface of said semiconductor chip toward four corners of said semiconductor chip.

55. (Once Amended) A semiconductor device comprising:

(1) a semiconductor chip having a main surface and a rear surface opposite to said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface;

(2) a lead frame including:

a chip mounting cross for mounting said semiconductor chip;

a plurality of suspension leads which are continuously formed with said chip mounting cross; and

a plurality of leads, said plurality of leads being arranged to extend toward said chip mounting cross;

(3) a plurality of bonding wires electrically connecting said plurality of leads with said plurality of bonding pads, respectively; and

(4) a resin body sealing said semiconductor chip, at least a portion of said plurality of leads, said chip mounting cross, said plurality of suspension leads and said plurality of bonding wires,

wherein said chip mounting cross has a first portion extending in a first direction and a second portion extending in a second direction which is a different direction from said first direction, said second portion intersecting said first portion,

wherein a width of at least a portion of each of said first and second portions of said chip mounting cross is wider than that of each of said plurality of suspension

leads,

wherein both ends of each of said first and second portions of said chip mounting cross are coupled with said plurality of suspension leads respectively,

wherein an intersecting portion of said first and second portions of said chip mounting cross is located at a substantially central portion of said rear surface of said semiconductor chip,

wherein said both ends of each of said first and second portions of said chip mounting cross are located at the peripheral portions of said rear surface of said semiconductor chip, and

wherein said rear surface of said semiconductor chip is fixed to said chip mounting cross and said both ends of each of said first and second portions at both of said central and peripheral portions of said rear surface of said semiconductor chip by an adhesive,

wherein said suspension leads and said chip mounting cross of said lead frame are continuously formed in an area of said semiconductor chip.

56. (Unamended) A semiconductor device according to Claim 55, wherein said first and second directions intersect each other at a substantially right angle.

57. (Unamended) A semiconductor device according to Claim 56, wherein said resin body has a tetragonal shape, wherein said plurality of leads extends toward four sides of said resin body, and wherein said plurality of suspension leads extend from said both ends of said first and second portions of said chip mounting cross toward four corners of said resin body.

58. (Unamended) A semiconductor device according to Claim 55, wherein a portion of said rear surface of said semiconductor chip is adhered to said first and second portions of said chip mounting cross, and wherein another portion of said rear surface of said semiconductor chip is contacted with said resin body.

59. (Unamended) A semiconductor device according to Claim 58, wherein said semiconductor chip has a tetragonal shape, and wherein said both ends of each of said first and second portions are located at the vicinity of four corners of said semiconductor chip.

60. (Unamended) A semiconductor device according to Claim 37, wherein said insulating tape has a closed frame shape.

61. (Unamended) A semiconductor device according to Claim 40, wherein said insulating tape has a closed frame shape.

62. (Unamended) A semiconductor device according to Claim 42, wherein said insulating tape has a closed frame shape.

REMARKS

This Amendment is responsive to the Office Action identified above, and is responsive in any other manner indicated below.

SUPPLEMENTAL REISSUE OATH/DECLARATION

The reissue oath/declaration has been objected to based upon the Office Action concern(s) as set forth within the Office Action. MPEP 1444's section II indicates that Applicant is able to defer the filing of a Supplemental Reissue Oath/Declaration until the end of prosecution). Applicant is **presently in the process of having the inventor(s) execute a Reissue Oath/Declaration** covering all presently-existing reissue errors and/or all papers submitted to date (including this paper), and such executed Reissue Oath/Declaration **will be submitted shortly**. That is, Applicant purposefully is having a Reissue Oath/Declaration executed subsequent to submission of this present Amendment, so that such Reissue Oath/Declaration can be comprehensive to cover amendments submitted (i.e., errors corrected) with this present Amendment, and **obviate any need for another supplemental Reissue Oath/Declaration**. If the Reissue Oath/Declaration becomes the only issue barring allowance of the application, the Examiner is asked to please refrain from issuing another action, and instead is invited to call the undersigned at the local Washington, D.C. telephone number of 703-312-6600 to provoke accelerated filing of such document to move the application to allowance.

WRITTEN CONSENT OF ASSIGNEE

The Written Consent Of Assignee has been objected to based upon the Office Action concern(s) as set forth within the Office Action. Traversal is appropriate. However, to travel a path of least resistance to grant of a patent, Applicant is **presently in the process of having the Assignee execute another Written Consent of Assignee (at the same time the Reissue Oath/Declaration mentioned above is being executed)** to cover amendments submitted (i.e., errors corrected) with this present Amendment, and **obviate any need for another supplemental Written Consent Of Assignee**. If the Written Consent Of Assignee becomes the only issue barring allowance of the application, the Examiner is asked to please refrain from issuing another action, and instead is invited to call the undersigned at the local Washington, D.C. telephone number of 703-312-6600 to provoke accelerated filing of the of such document to move the application to allowance.

PENDING CLAIMS

Claims 1-14 and 37-62 were pending, under consideration and subjected to examination in the Office Action. Appropriate claims have been amended, canceled and/or added (without prejudice or disclaimer) in order to adjust a clarity and/or focus of Applicant's claimed invention. That is, such changes are unrelated to any prior art or scope adjustment and are simply refocused claims in which Applicant is present interested. At entry of this paper, Claims 37-62 will be pending for further consideration and examination in the application.

REISSUE BROADENING – TWO-YEAR BAR

The section numbered "3" beginning on "Page 2" of at least the 14 May 2009 Office Action rejects claims 37-62 "...as being broadened in a reissue application filed outside the two year period." **Strong traversal is appropriate**.

More particularly, a portion of **MPEP Section 1412.03**, subsection "**IV WHEN A BROADENED CLAIM CAN BE PRESENTED**", page 1400-29, Rev. 7, July 2008, is reproduced and highlighted herewith, as follows:

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Thus, a broadened claim may be presented in a reissue application after the two years, even though the broadened claim presented after the two years is different than the broadened claim presented within the two years. Finally, if intent to broaden is indicated in a parent reissue application within the two years, a broadened claim can be presented in a continuing (continuation or divisional) reissue application after the two year period. In any other situation, a broadened claim cannot be presented, and the examiner should check carefully for the improper presentation of broadened claims.

A reissue application filed on the 2-year anniver-

Given that Applicant's parent (original) reissue application indicated an intent to, and did in fact, broaden within two years from the grant of the original patent, and given the fact that **Applicant claims 120 priority** from such parent (original) reissue application, it is respectfully submitted that **broadening is permitted** within the present application (whether it is a **CONTINUATION** application **or DIVISIONAL** application). Accordingly, reconsideration and withdrawal of any

rejection of Applicant's claim(s) based upon the two-year (2-year) broadening bar, are respectfully requested.

REJECTION UNDER '112, 2ND PAR. OBVIATED VIA CLAIM CANCELLATION

Claims 1-14 have been rejected under 35 USC '112, second paragraph, as being indefinite for the concerns listed on pages 3 and 4 of the Office Action. Care has been taken to now insure that patented claims 1-14 exist only within the parent Reissue application, i.e., any claim 1-14 have been removed from this related divisional Reissue application, and accordingly, any confusion or conflict with claims 1-14 of related parent Reissue applications has been obviated. As the foregoing is believed to have addressed all '112 second paragraph concerns, and withdrawal of the '112 second paragraph rejection are respectfully requested.

DOUBLE PATENTING REJECTION - TRAVERSED/NOT SUPPORTED

The non-statutory double patenting rejection is respectfully traversed because such rejection does not provide the factual analysis required for such rejections under U.S. patent law, i.e., the Examiner has not satisfied his/her initial burden to adequately support the rejection. More particularly, MPEP 804 providing guidance for examining states that

"Since the analysis employed in an obviousness-type double patenting determination parallels the guidelines for a 35 USC 103(a) rejection, the factual inquiries set forth in Graham v. John Deere Co., 383 US 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 USC 103 are employed when making an obviousness-type double patenting analysis. These factual inquiries are summarized as follows:

(A) Determine the scope and content of a patent claim and the prior art relative to a claim in the application at issue;

(B) Determine the differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue;

(C) Determine the level of ordinary skill in the pertinent art; and

(D) Evaluate any objective indicia of non-obviousness.

. . .

Any obviousness-type double patenting rejection should make clear:

(A) The differences between the invention defined by the conflicting claims - a claim in the patent compared to a claim in the application; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent."

The rejection does not make clear the differences, or the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent. That is, the Office Action comments have supplied only a bare conclusion, with no accompanying discussions of differences or obviousness reasons. Accordingly, Applicant respectfully submits that the above analysis should be provided in order for the Examiner to satisfy his/her initial burden to support the rejection, or the rejection should be withdrawn.

Despite the above traversal, it is respectfully submitted that such rejection has been rendered **obviated by the cancellation of allegedly double-patenting claims from the related reissue application(s)**. The above statements, or any present cancellation of disputed claims (without prejudice or disclaimer), should not be taken as an indication or admission that the objection or rejection was valid, or as a disclaimer of any scope or subject matter, but is merely use of a procedural approach to move toward a patent as quickly as possible.

EXAMINER INVITED TO TELEPHONE

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703/312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

RESERVATION OF RIGHTS

It is respectfully submitted that any and all claim amendments and/or cancellations submitted within this paper and throughout prosecution of the present application are without prejudice or disclaimer. That is, any above statements, or any present amendment or cancellation of claims (all made without prejudice or disclaimer), should not be taken as an indication or admission that any objection/rejection was valid, or as a disclaimer of any scope or subject matter. Applicant respectfully reserves all rights to file subsequent related application(s) (including reissue applications) directed to any/all previously claimed limitations/features which have been subsequently amended or cancelled, or to any/all limitations/features not yet claimed, i.e., Applicant continues (indefinitely) to maintain no intention or desire to dedicate or surrender any limitations/features of subject matter of the present application to the public.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the application is now in condition for allowance.

To the extent necessary, Applicant petitions for an extension of time under 37

CFR '1.136. Authorization is herein given to charge any shortage in the fees, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (Case No. 1374.32049RV2) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

/Paul J. Skwierawski/
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